BS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,866	05/02/2001	Behzad Razavi	20798-000110US	5822

27820 7590 11/15/2004

WITHROW & TERRANOVA, P.L.L.C.
P.O. BOX 1287
CARY, NC 27512

EXAMINER	
NGUYEN, DAVID Q	
ART UNIT	PAPER NUMBER
2681	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,866	RAZAVI ET AL.	
	Examiner	Art Unit	
	David Q Nguyen	2681	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *19-26 and 33-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,27-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 09/09/04 have been fully considered but they are not persuasive.

In response to Applicant's Remarks, on page 8, Applicants argue: "Graziadei fails to expressly or inherently disclose at least a mixer circuit comprising a gain stage coupled to receive a modulated bias current on a common node, the gain stage having a first current a current shunt circuit coupled between the common node and a reference voltage, the current shunt circuit having a second current, wherein the first current and the second current are coupled to the common node, and a bias circuit to generate the modulated bias current".

Examiner respectfully disagrees because Graziadei et al clearly shows and discloses a mixer circuit comprising a gain stage coupled to receive a modulated bias current on a common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15), the gain stage having a first current a current shunt circuit coupled between the common node and a reference voltage (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15), the current shunt circuit having a second current, wherein the first current and the second current are coupled to the common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15), and a bias circuit to generate the modulated bias current (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2,6,10-11,14-15,17-18,27-29 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Graziadei et al (US 4480337).

Regarding claim 1, Graziadei et al discloses a mixer circuit comprising: a gain stage coupled to receive a first signal on a first input (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15) and a modulated bias current on a common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15), and in accordance therewith, produce an output signal, the gain stage having a first current (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15); a current shunt circuit coupled between the common node and a reference voltage (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15), the current shunt circuit having a second current, wherein the first current and the second current are coupled to the common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15); and a bias circuit to generate the modulated bias current, the bias circuit having an input coupled to receive a second signal, and in accordance therewith, generate the modulated bias current, and an output coupled to the common node to provide the modulated bias current to the gain stage (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 2, Graziadei et al also discloses wherein the second current controls the gain of the gain stage and bias circuit (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 6, Graziadei et al also discloses wherein the second signal is an RF signal and the first signal is a differential signal (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15)

Regarding claims 10, Graziadei et al also discloses wherein the differential signal is generated by a local oscillator, and wherein the output of the local oscillator is amplified to generate a differential signal that approximates a square wave (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15)

Regarding claims 11, wherein the bias circuit comprises a first transistor having a control input and a first and second output, wherein the control input is coupled to receive an RF signal, the first output is coupled to a second reference voltage, and the second output is coupled to the common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 14, Graziadei et al also disclose wherein the gain stage is a differential stage and the first signal is a differential signal (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 15, Graziadei et al also discloses wherein the differential stage comprises: a first transistor having a control input and first and second outputs, the control input coupled to receive a first component of the differential signal; a second transistor having a control input and first and second outputs, the control input coupled to receive a second component of the differential signal; and a load coupled to the first output of the first transistor and to the first output of the second transistor, wherein the second output of the first transistor and the second output of the second transistor are coupled together and to the common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claims 17, Graziadei et al also discloses wherein the load comprises a first resistor coupled between the first output of the first transistor and a supply voltage and a second resistor coupled between the first output of the second transistor and the supply voltage (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 18, Graziadei et al also discloses wherein the reference voltage is a supply voltage (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 27-29 and 32, Graziadei et al discloses a method of mixing signals in a mixer circuit comprising: generating a first current in a differential stage; generating a second current in a shunt circuit coupled between the common node and a reference voltage (see fig. 2); coupling the first current and the second current through a common node to generate a bias current in a bias circuit; receiving an RF signal in the bias circuit; receiving a second signal in the differential stage; and generating a mixer output in accordance with the RF signal and the second signal (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15); modulating the bias current in accordance with the RF signal (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15); coupling the modulated bias current into the differential stage through the common node (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15); wherein the mixer output is proportional to the product of the first signal and the second signal (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-5,7-9,12-13,16 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Graziadei et al (US 4480337).

Regarding claim 3, Graziadei et al disclose a mixer comprising all of the limitations as claimed in claim 1. Graziadei et al fail to disclose the current shunt circuit comprises a MOS transistor coupled between the common node and the reference voltage. However, Graziadei et al discloses a transistor coupled between the common node and the reference voltage (see fig. 2). Official notice is taken that the MOS transistor of applicant's claimed invention is equivalent to the transistor of Graziadei et al's reference in order to use in the shunt circuit of the mixer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide above teaching to shunt the circuit of the mixer.

Regarding claims 4-5, Graziadei et al also discloses wherein the current shunt circuit comprises a MOS transistor coupled between the common node and the reference voltage; wherein the reference voltage is a supply voltage (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15); wherein current shunt circuit further comprises a resistor coupled in series between the common node and the MOS transistor.

Regarding claims 7-9, Graziadei et al does not mention wherein the frequency of the differential signal is an integer fraction of the frequency of the RF signal; wherein the integer fraction is one-third; wherein the differential signal is approximately a square wave. Official notice is taken that wherein the frequency of the differential signal is an integer fraction of the frequency of the RF signal; wherein the integer fraction is one-third; wherein the differential signal is approximately a square wave are well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide above teaching to design gain stage as desired design.

Regarding claim 12, Graziadei et al fails to disclose wherein the first transistor is an NMOS transistor. However, Graziadei et al discloses wherein the first transistor is a transistor (see fig. 2). Official notice is taken that the NMOS transistor of applicant's claimed invention is equivalent to the transistor of Graziadei et al's reference as desired design. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide above teaching to amplify an RF input as desired design.

Regarding claim 13, Graziadei et al also discloses wherein the bias circuit further comprises a capacitor having a first terminal coupled to the gate of the first transistor and a second terminal coupled to receive the RF input signal (see fig. 2 and col. 1, lines 57 to col. 4, line 24; col. 4, lines 9-15).

Regarding claim 16, Graziadei et al fails to disclose wherein the first and second transistors are NMOS transistors. However, Graziadei et al discloses wherein the first and second transistors are transistors (see fig. 2). Official notice is taken that the NMOS transistors of applicant's claimed invention are equivalent to the transistors of Graziadei et al's reference as

desired design. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide above teaching to amplify an RF input and to use in the shunt circuit as desired design.

Regarding claims 30-31, Graziadei et al does not mention wherein the frequency of the second signal is an integer fraction of the frequency of the RF signal; wherein the integer fraction is one-third. Official notice is taken that wherein the frequency of the differential signal is an integer fraction of the frequency of the RF signal; wherein the integer fraction is one-third are well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide above teaching to design gain stage as desired design.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Q Nguyen whose telephone number is 703-605-4254. The examiner can normally be reached on 8:30AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on 703-308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN

David Nguyen

DAVID HUDSPETH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600